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Qualcomm Incorporated
Patents Department
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EXAMINER
LIU, SHUWANG

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/723,795	EASTON ET AL.	
	Examiner	Art Unit	
	Shuwang Liu	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-34 and 36-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 7-13, 23-26, 32, 36-38, 40-49 and 54 are rejected under 35 U.S.C. 102(a) as being anticipated by Kawabe et al. (EP 0998052A2).

As shown in figures 1-10, Kawable et al. discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1 and 48:

a first buffer (203-1-3 in figure 1 or 402 in figure 5) operative to receive and store digitized samples at a particular sample rate (column 5, lines 44-55); and

a data processor (202 in figure 2 or 403 in figure 5) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate (column 5, lines 50-55, column 8, line 43-column 9, lines 13).

(2) regarding claim 2:

further comprising: a controller (401) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor (column 9, lines 28-36).

(3) regarding claim 3:

wherein the controller is operative to direct processing of the segments of digitized samples (column 9, lines 28-36).

(4) regarding claim 7:

further comprising: a receiver (201) operative to receive and process a transmitted signal to provide the digitized samples (column 4, lines 46-49 and column 5, lines 44-47).

(5) regarding claims 8 and 49:

wherein the data processor includes a correlator (208-1-n or 503 in figure 6) operative to despread the retrieved segments of digitized samples with corresponding

segments of PN despreading sequences to provide correlated samples (column 8, lines 5-9).

(6) regarding claim 9:

wherein the data processor further includes a symbol demodulation and combiner (214) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols (column 6, lines 9-21).

(7) regarding claim 10:

wherein the data processor further includes an accumulator (504 in figure 6, 904 in figure 7, 604 in figure 8, or 705 in figure 9) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

(8) regarding claim 11:

wherein the data processor further includes a second buffer (404) coupled to the symbol demodulation and combiner and operative to store the processed symbols (column 9, lines 40-53).

(9) regarding claim 12:

wherein the correlator includes a set of K multipliers (208-1, 208-2,... or 903-1, 903-2, .. in figure 7 or 704 in figure 9) operative to concurrently despread sets of up to K complex digitized samples (column 12, line 51-column 13, line 23).

(10) regarding claim 13:

wherein the correlator further includes a set of K summers (705) coupled to the set of K multipliers, each summer operative to receive and sum pairs of samples from two multipliers (column 12, line 51-column 13, line 23).

(11) regarding claim 23:

wherein the second buffer is operative to provide the processed symbols to a subsequent signal processing element (215 or 407)in an output order that is different from an input order to provide de-interleaving of the processed symbols (column 6, lines 22-25 and column 14, lines 3-15).

(12) regarding claim 24:

It is inherent that the second buffer includes at least two sections, one section operative to store processed symbols for a current packet (current slot) being processed and another section operative to store processed symbols for a prior processed packet (prior slot) to be provided to the subsequent signal processing element (column 9, lines 3-13).

(13) regarding claim 25:

wherein the accumulator is operative to accumulate the correlated samples over a programmable time interval to provide pilot signal estimates (column 12, lines 9-35).

(14) regarding claim 26:

wherein the accumulator includes a plurality of accumulate elements (504 and 505 in figure 7, or 904-1, 904-1, ...905-1, 905-2, ... in figure 7), each accumulate element operative to provide pilot signal estimate for a particular time offset (column 12, lines 9-35).

(15) regarding claim 32:

wherein the sample rate is asynchronous with the processing clock (column 9, lines 27-37).

(16) regarding claim 36:

further comprising: a data interface (201)coupled to the first buffer, the data interface operative to receive the digitized samples, discard unnecessary samples, and assemble the samples into words suitable for efficient storage to the first buffer.

(17) regarding claim 37:

wherein a word of 32 bits (for w-cdma) or more is written to the first buffer or read from the first buffer for each buffer access (column 4, line 54-column 5, line 355).

(18) regarding claim 38:

wherein the first buffer is operative to store two or more packets of digitized samples (column 4, line 54-column 5, line 55).

(19) regarding claim 40:

wherein multiple instances of the received signal are processed by retrieving and processing segments of digitized samples at multiple time offsets (column 4, line 54-column 5, line 55).

(20) regarding claim 41:

wherein at least one of the parameter values is programmable (column 11, line 57-column 12, line 7).

(21) regarding claim 42:

wherein the sample rate is twice a chip rate of the communications system (column 5, lines 44-55).

(22) regarding claim 43:

wherein the frequency of the processing clock is at least ten times higher than the sample rate (column 5, lines 44-55).

(23) regarding claim 44:

wherein the wireless communications system is a high data (HRD) CDMA system (WCDMA) (column 4, line 54-58 and column 5, lines 44-55).

(24) regarding claim 45:

A user terminal in a spread spectrum communications system comprising the receiver unit, of claim 1 (see receive side in figure 1).

(25) regarding claim 46:

A base station in a spread spectrum communications system comprising the receiver unit of claim 1 (see receive side in figure 1).

(26) regarding claims 47 and 54:

A receiver unit and a method for processing a received signal in a wireless communications system, comprising:

a receiver (see receiver side in figure 1) operative to receive and process a transmitted signal to provide digitized samples at a particular sample rate;

a first buffer (203-1-3 in figure 1 or 402 in figure 5) coupled to the receiver and operative to receive and store the digitized samples (column 5, lines 44-55);

a data processor (202 in figure 2 or 403 in figure 5) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher

than the sample rate (column 5, lines 50-55, column 8, line 43-column 9, lines 13), and wherein the data processor includes

a correlator (208-1-n or 503 in figure 6) operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples (column 8, lines 5-9),

a symbol demodulation and combiner (214) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols, a second buffer coupled to the symbol demodulation and combiner and operative to store the processed symbols (column 6, lines 9-21), and

an accumulator (504 in figure 6, 904 in figure 7, 604 in figure 8, or 705 in figure 9) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results; and

a controller (401) coupled to the data processor and operative to dispatch tasks for the data processor and to process the accumulated results from the data processor (column 9, lines 28-36).

3. Claims 1, 2, 8-10, 36, 47-49 and 54 are rejected under 35 U.S.C. 102(a) as being anticipated by Lee (EP 1017183A2).

As shown in figures 1-6, Lee discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1 and 48:

a first buffer (322 in figure 3) operative to receive and store digitized samples at a particular sample rate (column 6, lines 10-30); and

a data processor (320 in figure 3) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate (column 6, lines 10-30, column 3, line 14-column 4, 29, claims 1 and 9).

(2) regarding claim 2:

further comprising: a controller (114 in figure 1 or 316 in figure 3) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor.

(3) regarding claims 8 and 49:

wherein the data processor includes a correlator (404 in figure 4 or 600-604 in figure 6) operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples.

(4) regarding claim 9:

wherein the data processor further includes a symbol demodulation and combiner (608 and 612 in figure 6) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols (column 6, lines 9-21).

(5) regarding claim 10:

wherein the data processor further includes an accumulator (610 and 614 in) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results.

(5) regarding claim 39:

wherein the first buffer is further operative to store PN samples used for despreading the digitized samples (column 3, lines 44-7 and column 6, lines 10-30).

(6) regarding claims 47 and 54:

A receiver unit and a method for processing a received signal in a wireless communications system, comprising:

a receiver (102 and 106) operative to receive and process a transmitted signal to provide digitized samples at a particular sample rate;

a first buffer (322) coupled to the receiver and operative to receive and store the digitized samples (column 6, lines 10-30);

a data processor (320 in figure 3) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate ((column 6, lines 10-30, column 3, line 14-column 4, 29, claims 1, 9 and 22) wherein the data processor includes

a correlator (404 in figure 4 or 600-604 in figure 6) operative to despread the retrieved segments of digitized samples with corresponding segments of PN despreading sequences to provide correlated samples,

a symbol demodulation and combiner (608 and 612 in figure 6) coupled to the correlator and operative to receive and process the correlated samples to provide processed symbols, a second buffer coupled to the symbol demodulation and combiner and operative to store the processed symbols (column 6, lines 9-21), and

an accumulator (610 and 614 in figure 6) coupled to the correlator and operative to receive and process the correlated samples to provide accumulated results; and

a controller (114 in figure 1 or 316 in figure 3) coupled to the data processor and operative to dispatch tasks for the data processor and to process the accumulated results from the data processor.

4. Claims 1, 2, 29-31, 48 and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Bottomley (US 6,442,154).

As shown in figures 9 and 10, Bottomley discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1 and 48:

a first buffer (132) operative to receive and store digitized samples at a particular sample rate (column 8, lines 18-20; and

a data processor (102 and 134) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is

operated based on a processing clock having a frequency that is higher than the sample rate (column 9, lines 24-33).

(2) regarding claim 2:

further comprising: a controller (94, 96, 100 and 136) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor.

(3) regarding claim 29:

wherein the controller is operative to receive a timing signal (from 94) and initiate processing of the segments of digitized samples in response to the received timing signal (column 6, line 61-column 7, line 20 and column 8, lines 23-32).

(4) regarding claim 30:

wherein the timing signal is generated based on a comparison value (correlations) provided by the controller (column 7, lines 42-46).

(5) regarding claim 31:

wherein the timing signal is indicative of a particular number of digitized samples having been stored to the first buffer because the timing signal controls the subsample (see 92).

(6) regarding claim 53:

wherein the sample rate is asynchronous with the processing clock, the method further comprising: tracking a chip rate of the digitized samples (128 in figure 8); and providing a signal (output from 136) used to write digitized samples to the first buffer starting at designated locations.

5. Claims 1, 2, 33, 34 and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Kindred et al. (US 5,710,784).

As shown in figures 5 and 7, Bottomley discloses a receiver unit and a method for processing a received signal in a wireless communications system, comprising:

(1) regarding claims 1 and 48:

a first buffer (48 in figure 5 and 72 in figure 7) operative to receive and store digitized samples at a particular sample rate (column 8, lines 5-11; and

a data processor (50 in figure 5) coupled to the first buffer and operative to retrieve segments of digitized samples from the first buffer and to process the retrieved segments with a particular set of parameter values, wherein the data processor is operated based on a processing clock having a frequency that is higher than the sample rate (column 8, line 12-column 9, line 47).

(2) regarding claim 2:

further comprising: a controller (62 in figure 5) coupled to the data processor and operative to dispatch tasks for the data processor and to process signaling data from the data processor (column 8, lines 29-35).

(3) regarding claim 33:

further comprising a micro-controller (76 in figure 7) coupled to the controller and operative to receive the dispatched tasks and to generate a set of control signals to direct the operation of the first buffer and the data processor to execute the dispatched tasks (column 11, line 12-column 13, line 39).

(4) regarding claim 34:

wherein the micro-controller is operative to instantiate a task state machine for each task being processed (column 12, lines 8-65).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-6, 14, 16-22, 27, 28 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabe et al. in view of Subramanian et al. (US 6,459,883).

(1) regarding claims 4-6, 27 and 28:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the controller operating to instantiate a timing state machine for each signal instance being processed, wherein state machine includes a time tracking loop operative to track movement of the signal instance being processed as recited in the claims.

Subramanian et al., in the same field of endeavor, teaches a controller (116, 118, 120 and 122 in figure 1) having a timing state machine includes a time tracking loop operative to track movement of the signal instance being processed (abstract, column 3, lines 1-55, figures 8-12).

It would be desirable to provide a flexible and programmable generic rake receiver architecture suitable for different spread spectrum system at a minimal development cost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use controller as taught by Subramanian et al. to implement the controller of Kawabe et al. in order to provide an integration of generic, inexpensive components in a fully configurable manner.

(2) regarding claims 16-20 and 50:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the demodulator including a decover element operative to receive and decover the correlated samples with one or more Walsh codes to provide decovered symbols.

Subramanian et al., in the same field of endeavor, teaches a dechannelizer (110-114 in figure 1, 708, 710 in figure 7 and 928, 930 and 932 in figure 9) to decover the correlated symbols with Walsh codes (711), wherein the decover is implemented with a FHT (column 8, lines 40-45) operating for inphase and quadrature samples (see figure 7). Furthermore, it is inherent for WCDMA that the FHT element is operative to perform decovering with one or more Walsh symbols of a length of 1, 2, 4, 8, 16, 32, 64, or 128.

Although Kawable did not teach orthogonal Walsh channelization, Subrammanian et al. teach using dechannelization means by orthogonal Walsh code for separate channels (110-114 in figure 1 and figure 7). It is also well known that the orthogonal sequences currently used in CDMA system are Walsh codes of length 64. Walsh codes are used in forward CDMA link to separate users. In any given sector,

each forward code channel is assigned a distinct Walsh code. The receiver despreads the chips by using the same Walsh code used at the transmitter so that the symbols or digits are recovered without any error. When the wrong Walsh sequence is used for dispreading, the resulting correlation yields an average of zero. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use orthogonal Walsh code as taught by Subrammanian et al. in the demodulator of Kawable to perform the channelization in the CDMA receiver. In so doing, the receiver facilitates separating different users from the composite spread signal so that the channel security is improved and the data can be recovered without errors.

(3) regarding claims 21, 22, 51 and 52:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the demodulator including a pilot demodulator coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols.

Subramanian et al., in the same field of endeavor, teaches a pilot demodulator (figure 10) coupled to the decover element and operative to demodulate the decovered symbols with pilot symbols to provide demodulated symbols (column 8, line 64-column 8, line 18). Furthermore, Subramanian et al. teaches the demodulator including a symbol accumulator (1012) coupled to the pilot demodulation and operative to accumulate the demodulated symbols from multiple signal instances to provide the processed symbols (column 9, lines 19-27).

It is also well known that the pilot signals are used in transmission protocols to help the receiver estimate an unknown channel. If the transmitter sends out a known pilot signal with a known PN sequence, then the receiver can determine the phase correction using an internally generated PN sequences that is identical to that of the transmitter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use pilot signal as taught by Subrammanian et al. in the demodulator of Kawable to determine phase estimation and correction in the CDMA receiver. In so doing, the receiver facilitates separating different users from the composite spread signal so that the channel security is improved and the data can be recovered without errors.

(4) regarding claim 14:

Kawabe et al. discloses all of the subject matter as described above except for specifically teaching the correlator including an interpolator operative to receive and interpolate despread samples from the PN despreading to generate interpolated samples that are provided as the correlated samples.

Subramanian et al., in the same field of endeavor, teaches the correlator (910 and 902 in figure 9) includes an interpolator (902).

It should be noted that the arrangement of the blocks in Subramanians' correlator differs from claim 12 of the present invention. Subramanian et al. reversed the order of the despreader (910) and interpolator (902) recited. The order of despreader and interpolator does not affect the result of the output of the correlator because the two arrangements are art-recognized functional equivalents.

The interpolator is conventionally known in the art and discussed in John G. Proakis, Digital Communications, 2nd edition, McGraw-Hill, 1989. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the interpolator as taught by Subrammanian et al. in the correlator of Kawable to adjust the timing of the correlated signal. In so doing, the receiver facilitates timing adjustment from the spread signal so that the data can be recovered without errors.

Allowable Subject Matter

8. Claims 15 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach and suggest the receiver comprises the interpolator including one or more pairs of scaling elements, each scaling element operative to receive and scale respective despread samples with a particular gain to generate scaled samples, and one or more summer, each summer coupled to a respective pair of scaling elements and operative to receive and sum the scaled samples from the pair of scaling elements to generate the interpolated samples as received in claim 15. Furthermore, the prior art fails to teach and suggest the receiver comprises the micro-controller includes a set of latches operative to latch a dispatched task and one or more parameter values to be applied for the dispatched task, at least one counter, each

counter coupled to a respective latch and operative to provide an indicator signal based on a value stored in the latch, and a sequencing controller operative to receive at least one indicator signal and the dispatched task and to generate the set of control signals as recited in claim 35.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shuwang Liu whose telephone number is (703) 308-9556.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Shuwang Liu
Primary Examiner
Art Unit 2634

May 1, 2003